WHAT IS CLAIMED IS:

1. A register setting method for setting operation condition information, which defines the operation of a device, in a first register and a second register, the method comprising the steps of:

storing first operation condition information in the first register;

storing second operation condition information in the second register;

changing the first operation condition information; and

when the first operation condition information is changed, changing the second operation condition information in accordance with change information for changing the first operation condition information.

2. The register setting method according to claim 1, wherein:

the device generates a start signal for starting the device; and the method further comprising the step of:

loading the second operation condition information stored in the second register into the first register in response to the start signal.

3. The register setting method according to claim 1, wherein:

the first register generates a device control signal for controlling the operation of the device, the device control signal including the change information; and

the step of changing the second operation condition information includes the steps of:

detecting a change in the device control signal; and

when a change in the device control signal is detected, storing second operation condition information in the second register in response to the device control signal, the second operation condition information being identical to changed first operation condition information.

4. The register setting method according to claim 3, wherein:

the device generates a start signal for starting the device; and

the method further comprises the step of:

loading the first register with the second operation condition information stored in the second register in response to the start signal.

5. The register setting method according to claim 1, wherein:

the first register receives a set signal including the change information; and

the step of changing the second operation condition information includes the steps of:

detecting a change in the first operation condition information stored in the first register; and

when a change in the first operation condition information is detected, storing information identical to changed first operation condition information in response to the set signal.

6. The register setting method according to claim 5, wherein:

the device generates a start signal for starting the device; and

the method further comprises the step of:

loading the first register with the second operation condition information stored in the second register in response to the start signal.

7. The register setting method according to claim 6, wherein:

the first register receives a mode set signal including the mode change information, and generates a device control signal for controlling an operation mode of the device, the device control signal including the mode change information; and

the step of changing the second operation condition information includes the steps of:

detecting a change in the first operation condition information stored in the first register; and

when a change in the first operation condition information is detected, storing information identical to changed first operation condition information in the second register in response to the device control signal.

8. The register setting method according to claim 7, wherein:

the device generates a start signal for starting the device; and

the method further comprising:

loading the first register with the second operation condition information stored in the second register in response to the start signal.

9. A register setting method for setting operation condition information, which defines the operation of a device, in a first register including a volatile memory and a second register including a non-volatile memory, the

method comprising the steps of:

storing first operation condition information in the first register;

storing second operation condition information in the second register;

changing the second operation condition information; and

when the second operation condition information is changed, changing the first operation condition information in the first register substantially at the same time the second operation condition information is changed, in accordance with change information for changing the second operation condition information.

10. A semiconductor device having a plurality of operation modes and adapted to operate in accordance with operation condition information which defines each operation mode, the semiconductor device comprising:

a first register for storing first operation condition information;

a second register connected to the first register for storing second operation condition information; and

a device control circuit connected to the first register for controlling the operation of the semiconductor device in accordance with the first operation condition information or the second operation condition information,

wherein when the first operation condition is changed, the second register receives a set signal including change information for changing the first operation condition information, and changes the second operation condition information to changed first operation condition information in accordance with the change information.

11. The semiconductor device according to claim 10, wherein:

the first register includes a volatile memory, the volatile memory storing the first operation condition information; and

the second register includes a non-volatile memory, the non-volatile memory storing the second operation condition information.

12. The semiconductor device according to claim 10, wherein:

the semiconductor device generates a start signal for starting the device; and

the second register receives the start signal, and loads the first register with the second operation condition information in response to the start signal.

13. A semiconductor device having a plurality of operation modes and adapted to operate in accordance with operation condition information which defines each operation mode, the device comprising:

a first register for storing first operation condition information;

a change detector connected to the first register for detecting a change in the first operation condition information stored in the first register to generate a detection signal in accordance with the detected change;

a second register connected to the first register and the change detector for storing second operation condition information in response to the detection signal; and

a device control circuit connected to the first register for controlling the operation of the

semiconductor device in accordance with the first operation condition information or the second operation condition information,

wherein the second register receives a second register change signal including change information for changing the first operation condition information, and changes the second operation condition information to changed first operation condition information in accordance with the change information in response to the detection signal.

14. The semiconductor device according to claim 13, wherein:

the second register includes a rewrite control circuit for instructing rewriting of the second operation condition information in response to the detection signal.

15. The semiconductor device according to claim 14, wherein:

the rewrite control circuit receives an external command for rewriting the second operation condition information, and instructs the rewriting in accordance with the external command.

16. The semiconductor device according to claim 13, wherein:

the first register includes a volatile memory, the volatile memory storing the first operation condition information; and

the second register memory includes a non-volatile memory, the non-volatile memory storing the second operation condition information.

17. The semiconductor device according to claim 13, wherein:

the semiconductor device generates a start signal for starting the device; and

the second register receives the start signal, and loads the first register with the second operation condition information in response to the start signal.

18. The semiconductor device according to claim 13, wherein:

the first register receives a set signal including the change information, and changes the first operation condition information in accordance with the change information, the set signal being associated with the second register change signal; and

the change detector generates the detection signal in accordance with a detected change in the first operation condition information stored in the first register.

19. The semiconductor device according to claim 18, wherein:

the second register change signal comprises an address signal, which is supplied to the semiconductor device together with a control signal for decoding the plurality of operation modes.

20. The semiconductor device according to claim 13, wherein:

the second register change signal comprises the device control signal;

the first register receives a set signal including the change information and changes the first operation condition information in accordance with the change

information, and the first register further generates a device control signal including the change information and supplies the device control signal to the second register; and

the change detector generates the detection signal in accordance with a detected change in the first operation condition information stored in the first register.

21. The semiconductor device according to claim 13, wherein:

the second register change signal comprises the device control signal;

the first register receives a set signal including the change information, and changes the first operation condition information in accordance with the change information, and the first register further generates a device control signal including the change information and supplies the device control signal to the second register; and

the change detector detects a change in the device control signal, and generates the detection signal in accordance with a detected change in the device control signal.

22. A semiconductor device having a plurality of operation modes and adapted to operate in accordance with operation condition information which defines each operation mode, the device comprising:

a first register including a volatile memory for storing first operation condition information;

a second register connected to the first register and including a non-volatile memory for storing second operation condition information; and

a device control circuit connected to the first register and the second register for controlling the operation of the semiconductor device in accordance with the first operation condition information or the second operation condition information,

wherein when the second operation condition information is changed, the second register changes the first operation condition information in the first register to changed second operation condition information substantially at the same time the second operation condition information is changed, in accordance with change information for changing the second operation condition information.

23. The semiconductor device according to claim 22, wherein:

the second register includes a rewrite control circuit for controlling rewriting of the second register in accordance with an external command for rewriting the second operation condition information, wherein the rewrite control circuit controls rewriting of the first register.